

REMARKS

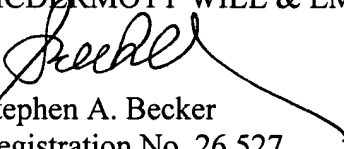
The above-referenced application has been amended to correct a minor informality with regards to the reference numbers in the specification and the drawings.

No new matter has been added.

Entry of this amendment is respectfully requested.

Respectfully submitted,

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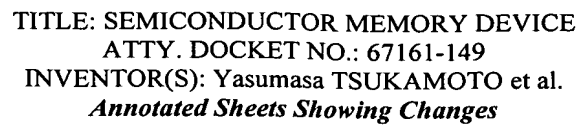


FIG. 1 is a plan view of a semiconductor device. The device is divided into three main regions: 40:NMOS REGION, 41:PMOS REGION, and 42:NMOS REGION. A central channel region (41) is flanked by NMOS regions (40 and 42). A dashed line indicates a cross-section L10. Various components are labeled: 50, 51, 52, 53, 54, 55, 60, 61, 62, 63, CN1, CN2, CN3, CN4, and L10.

A cross-sectional view of a CMOS device structure. The diagram shows a P SUBSTRATE at the base. Above it are alternating N WELL and P WELL regions. On top of these wells are NMOS and PMOS transistors, respectively. The NMOS gate is labeled 62, and the PMOS gate is labeled 61. A horizontal arrow at the top indicates the MEMORY CELL ONE-BIT WIDTH. Various reference numerals are placed along the bottom: 66, 40, 71, 70, 41, 72, 70, 42, 73, 67.

[illegible][illegible]